

Model Name: 8I945GME Revision 1.0

SHEET TITLE

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03	BOM & PCB MODIFY HISTORY
04	P4_LGA775_A
05	P4_LGA775_B
06	P4_LGA775_C
07	P4_LGA775_D,E,F,G
08	GMCH-LAKEPORT_HOST
09	GMCH-LAKEPORT_DDRII
10	GMCH-LAKEPORT_PCI E, DMI
11	GMCH-LAKEPORT_INT VGA
12	GMCH-LAKEPORT_GND
13	GMCH-LAKEPORT_PWR
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15	DDRII CHANNEL B 2
16	DDRII TERMINATION
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18	ICH7 PCI, USB, DMI, LAN
19	ICH7 IDE, GPIO, SATA, CTRL
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21	GB/CK410M CLOCK.
22	PCI SLOT 1,2,3
23	IDE/FLOPPY
24	ITE 8712 GBIX
25	COM_LPT
26	BIOS,CI,HWM,KB/MS
27	AC97 ALC655

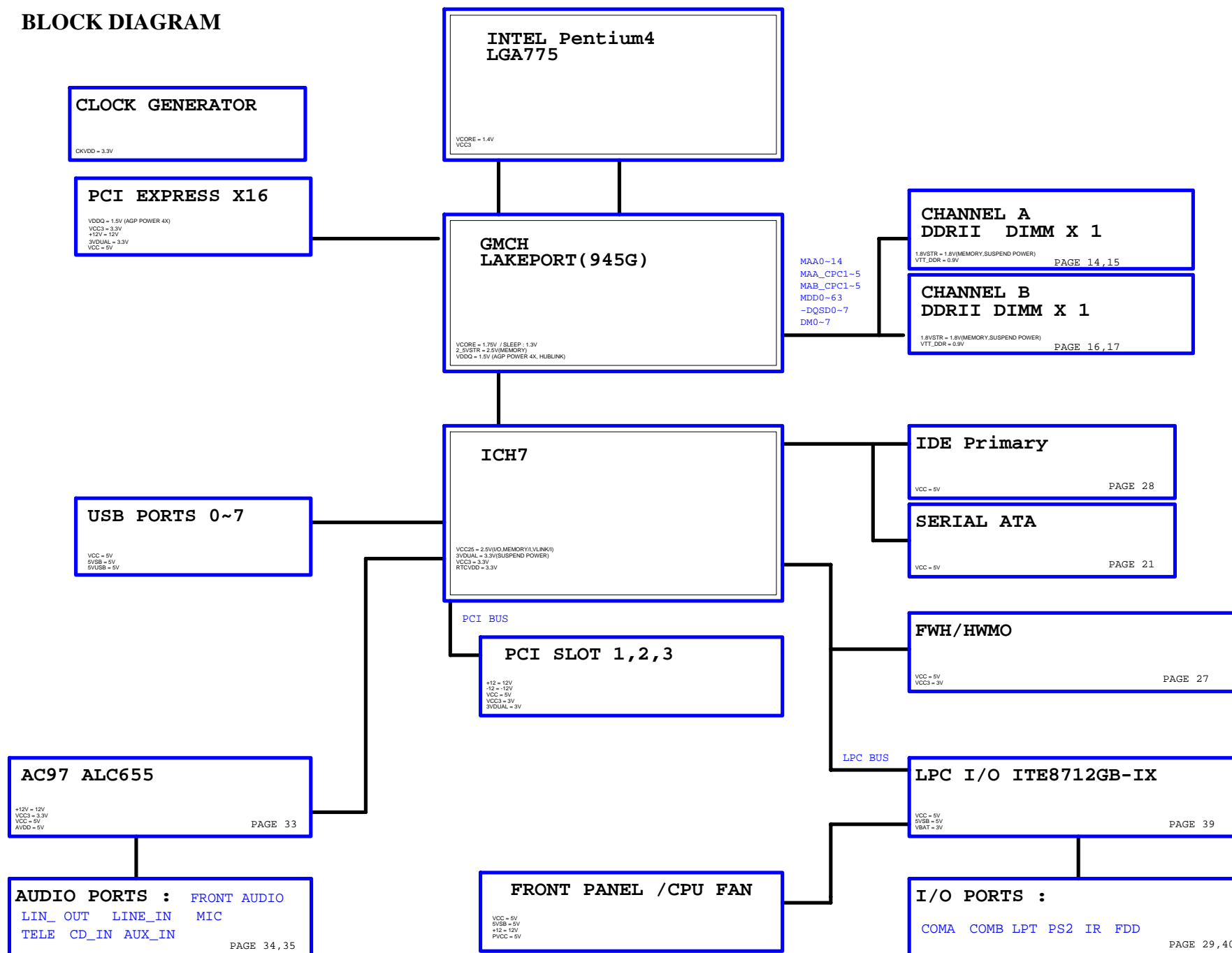
SHEET TITLE

28	REAR AUDIO JACK
29	DISCRETE POWER
30	VCORE PWM_ISL6556
31	ATX, OTHERS POWER
32	RTL8110S/RTL8100C
33	FRONT PANEL

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BLOCK DIAGRAM



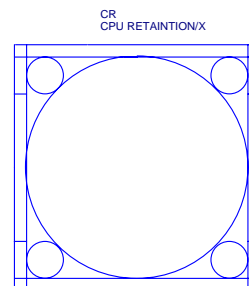
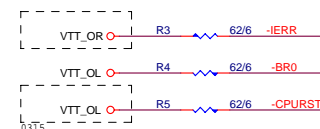
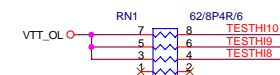
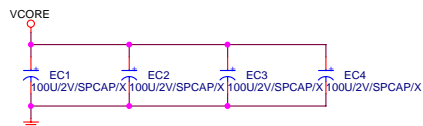
Version: 1.0

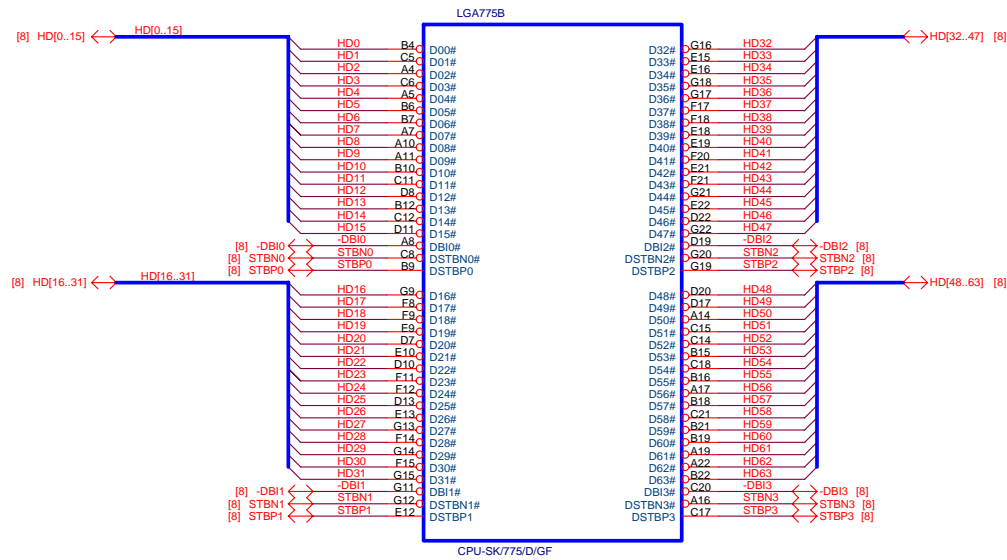
2005/10/26

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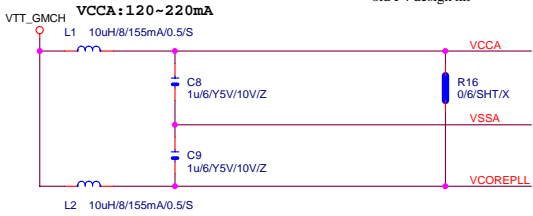
Circuit or PCB layout change
for next version

[illegible]



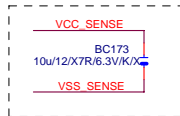
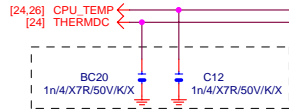
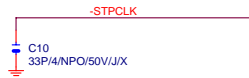


Note:
VCCA & VCCOREPLL
define doesn't same as
old P4 design kit



Trace width doesn't
less than 12 Mil

As close as possible to
CPU socket



945 Design Guide rev1.5 spec.
VCCA=120~220mA
公板爲125mA

10LI2-12100A-03=INDUCTOR 10uH 300mA TAI-TECH
10LI2-12100A-02=INDUCTOR 10uH 155mA TAIYO
10LI2-12100A-01=INDUCTOR 10uH 120mA TDK

限用兩種

CPU

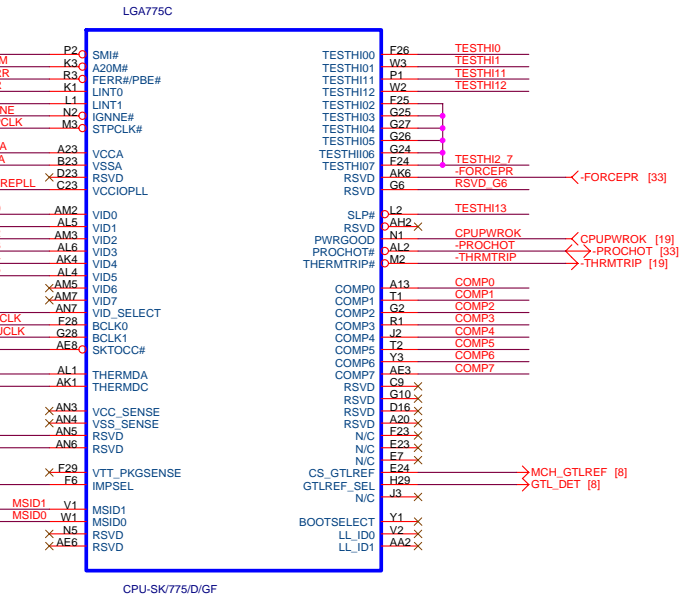
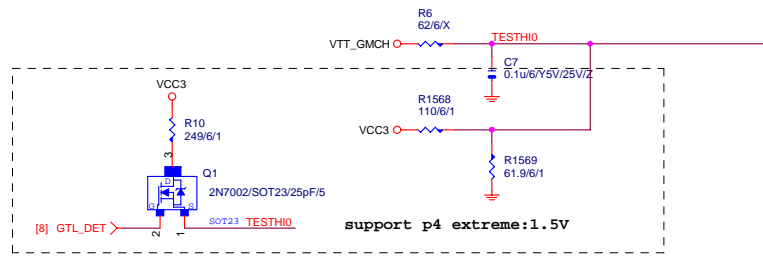
FSA	FSB	NA	Clock
FSBSEL0	FSBSEL1	FSBSEL3	Clock
1	0	1	100MHz
1	0	0	133MHz
1	1	0	166MHz
0	1	0	200MHz
0	0	0	266MHz

RATIO

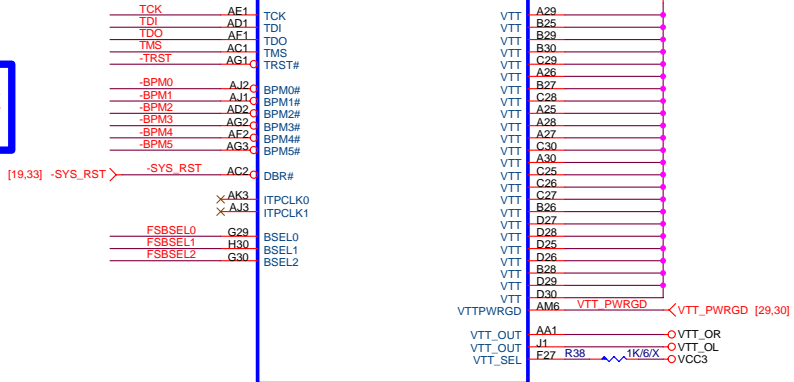
2.66/3.33

2.00/2.5

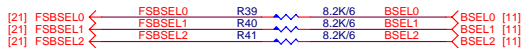
X



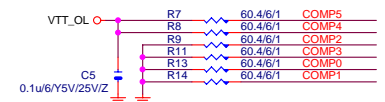
LGA775D



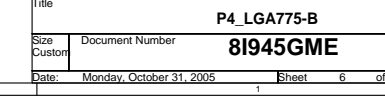
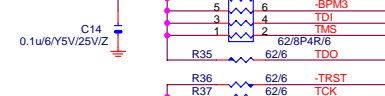
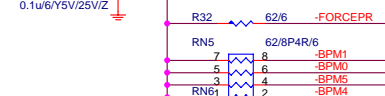
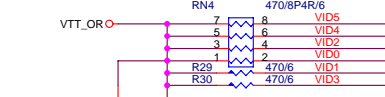
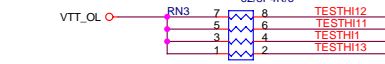
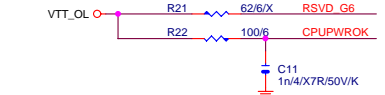
CPU-SK/775/D/GF



Place outside of CPU socket



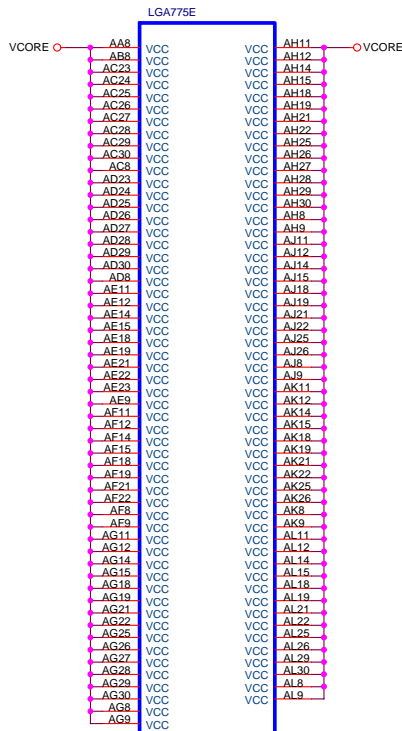
Locate at ICH7 Side



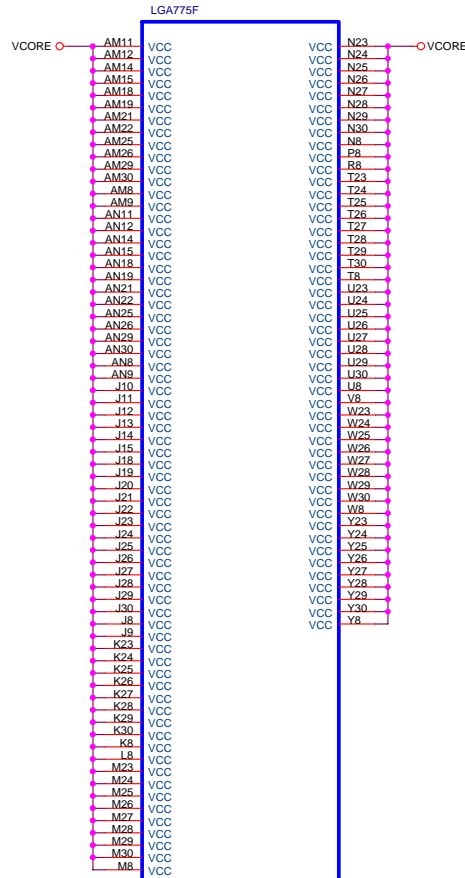
Gigabyte Technology

P4_LGA775-B

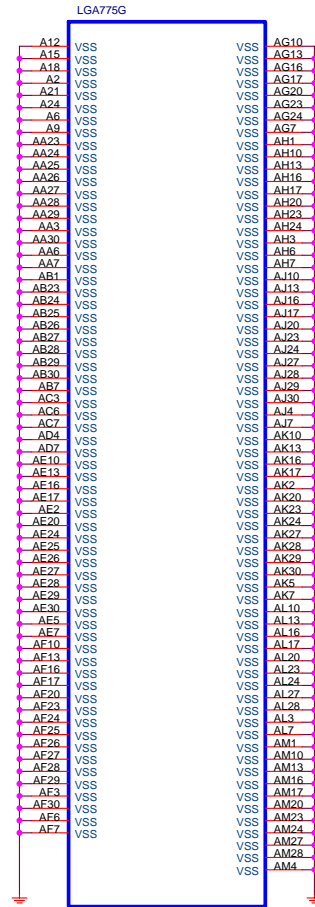
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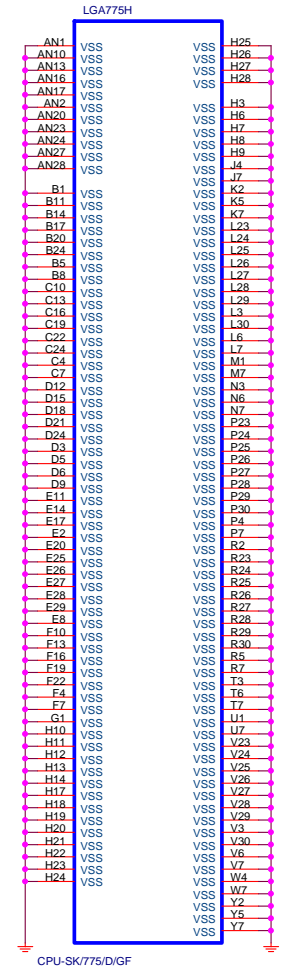
CPU-SK/775/D/GF



CPU-SK/775/D/GF



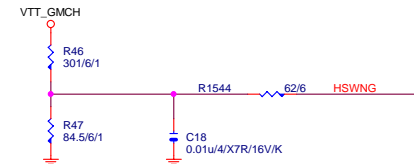
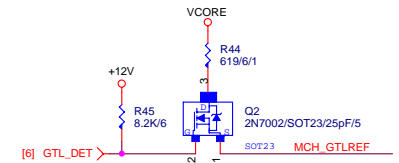
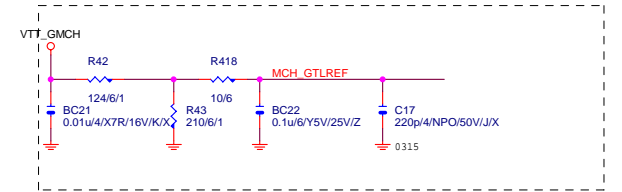
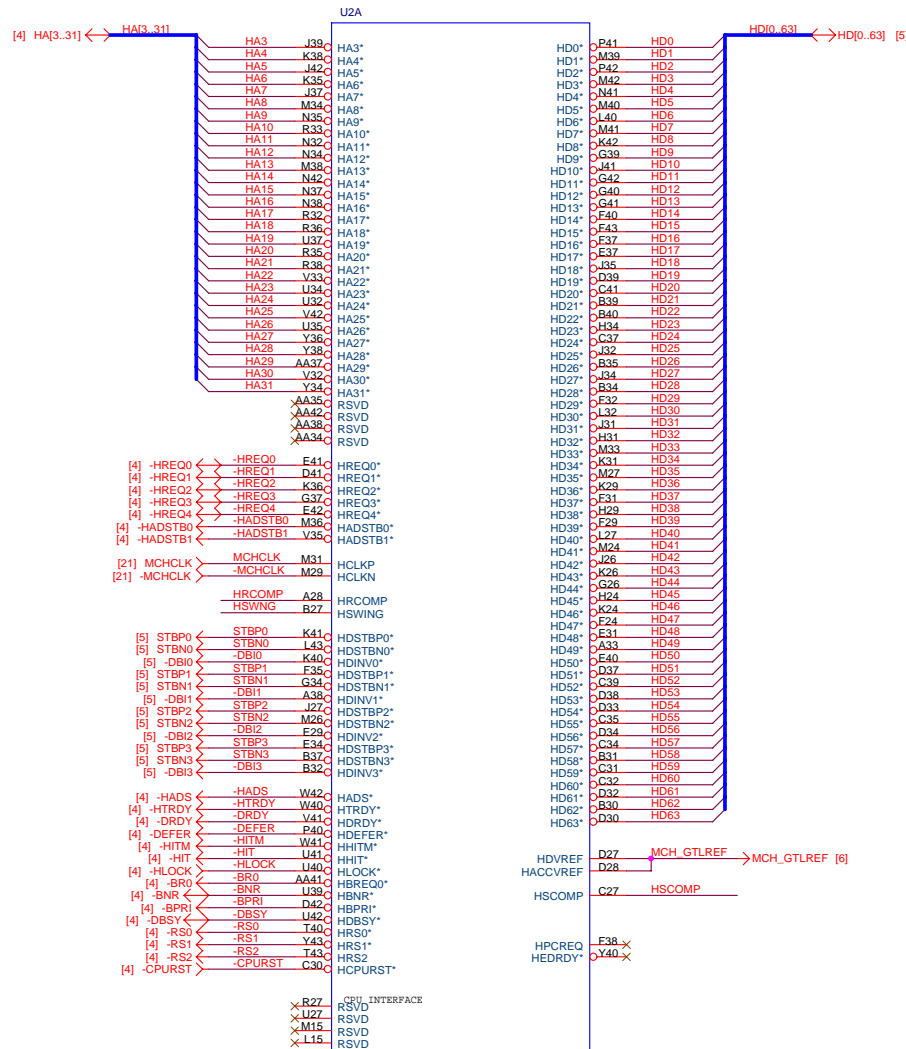
CPU-SK/775/D/GF



CPU-SK/775/D/GF

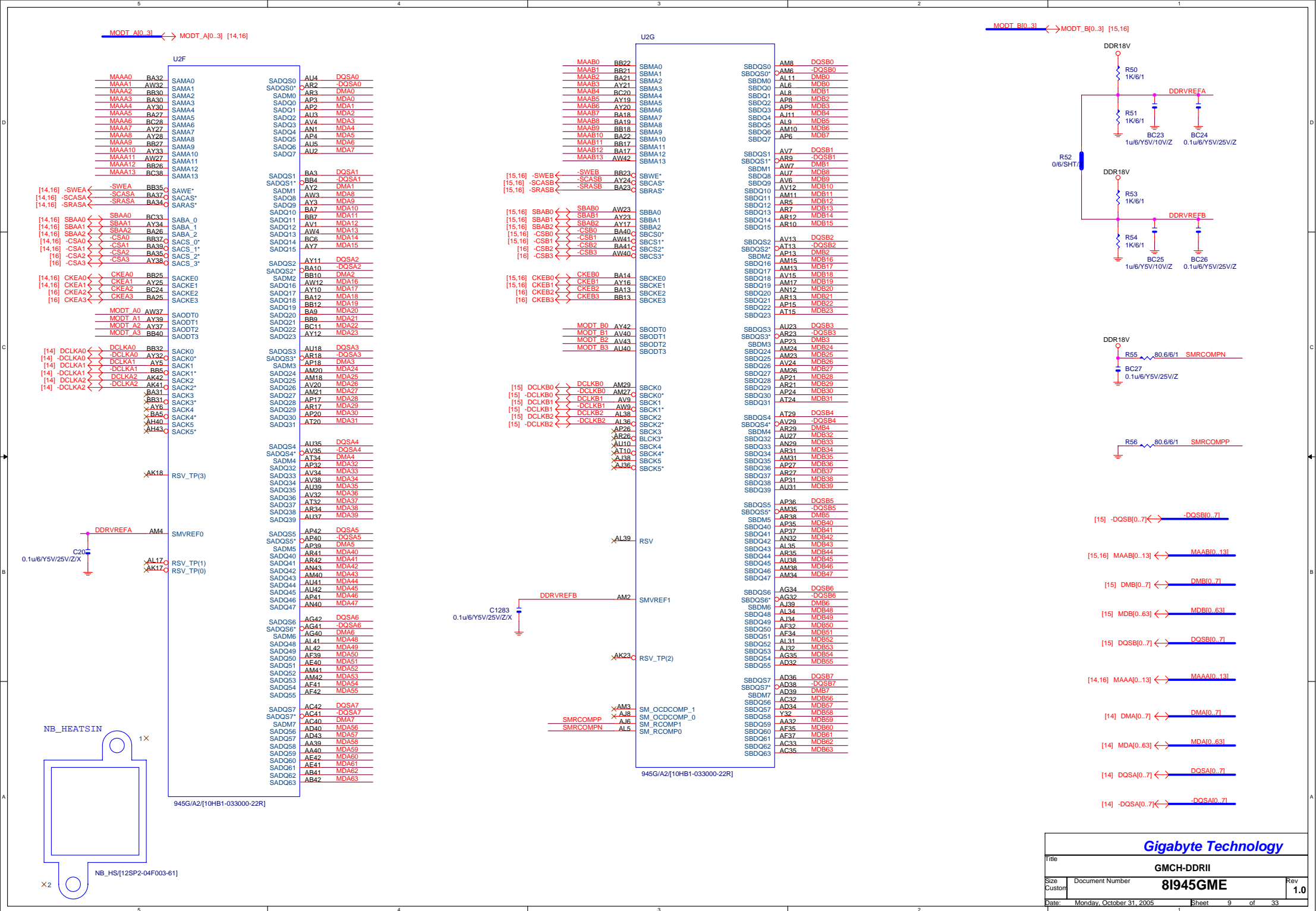
Gigabyte Technology

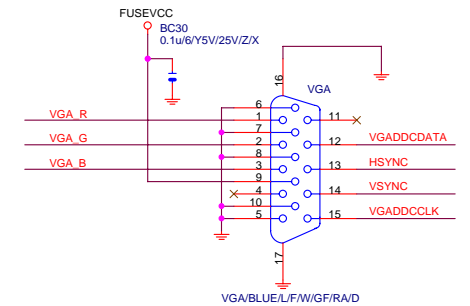
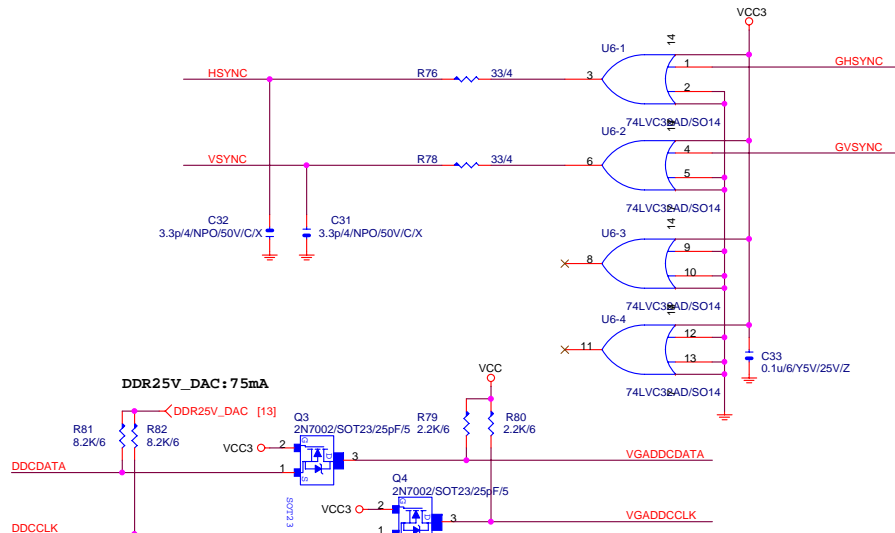
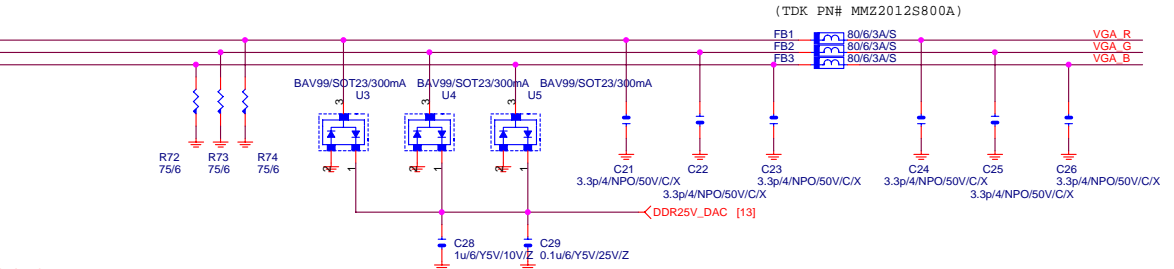
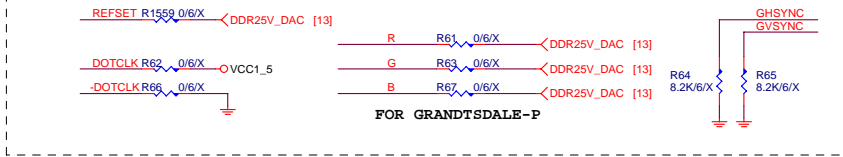
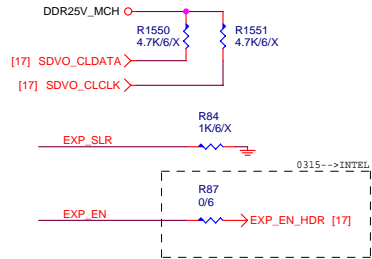
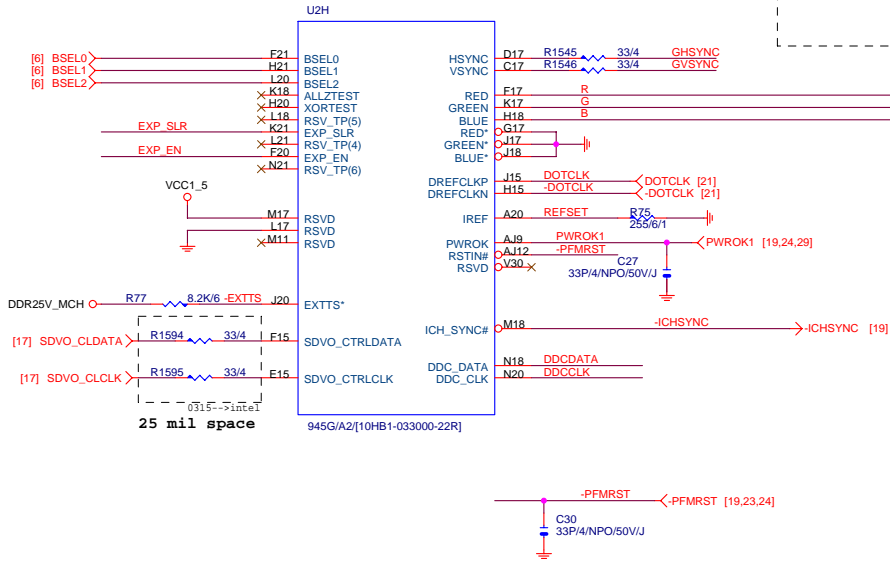
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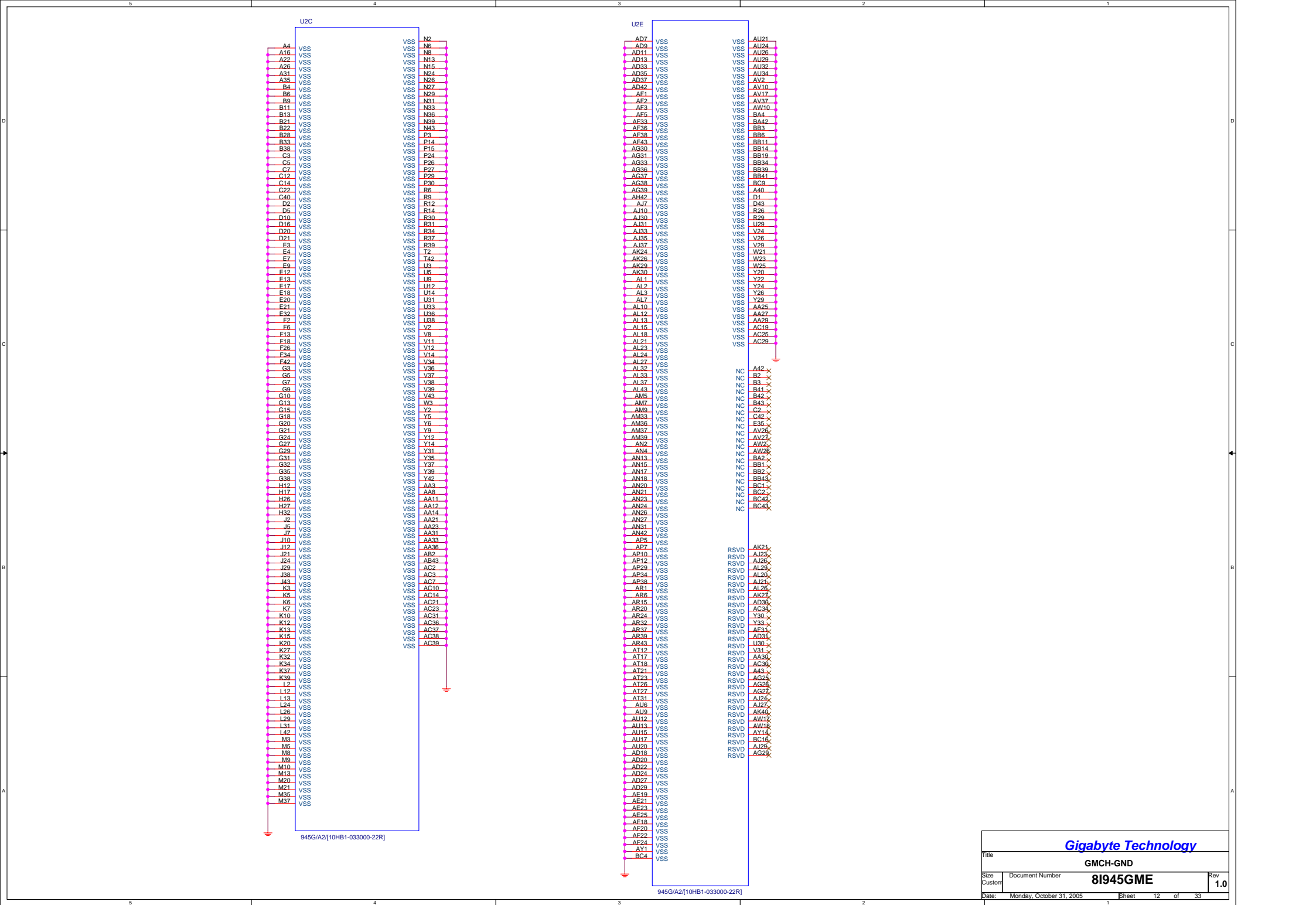


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Title			
GMCH-HOST			
Size	Document Number	81945GME	
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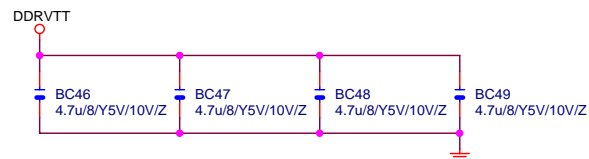






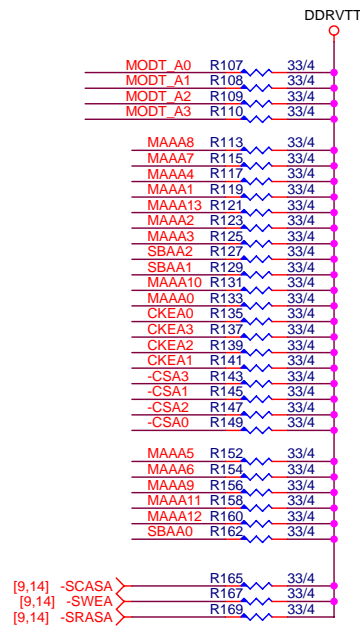
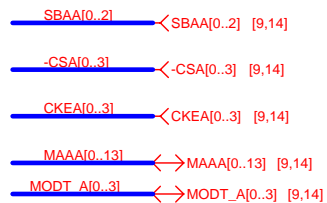
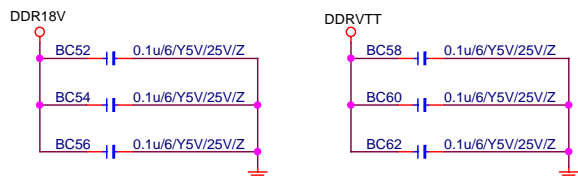
DDR TERMINATION CHANNEL A

DDRVTT Decouple



DDR18V Decouple

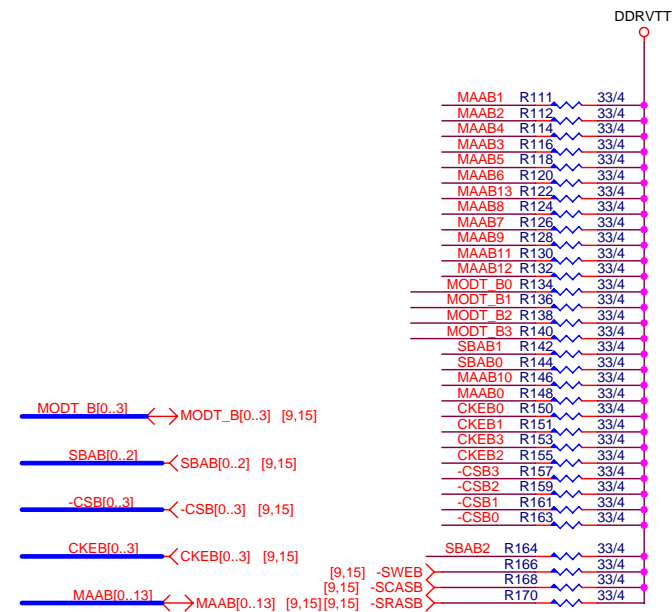
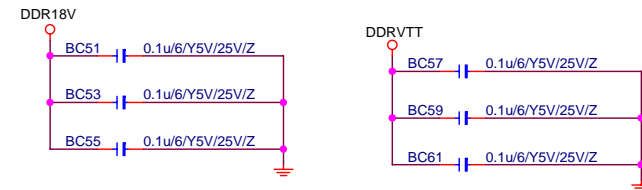
DDRVTT Decouple



DDR TERMINATION CHANNEL B

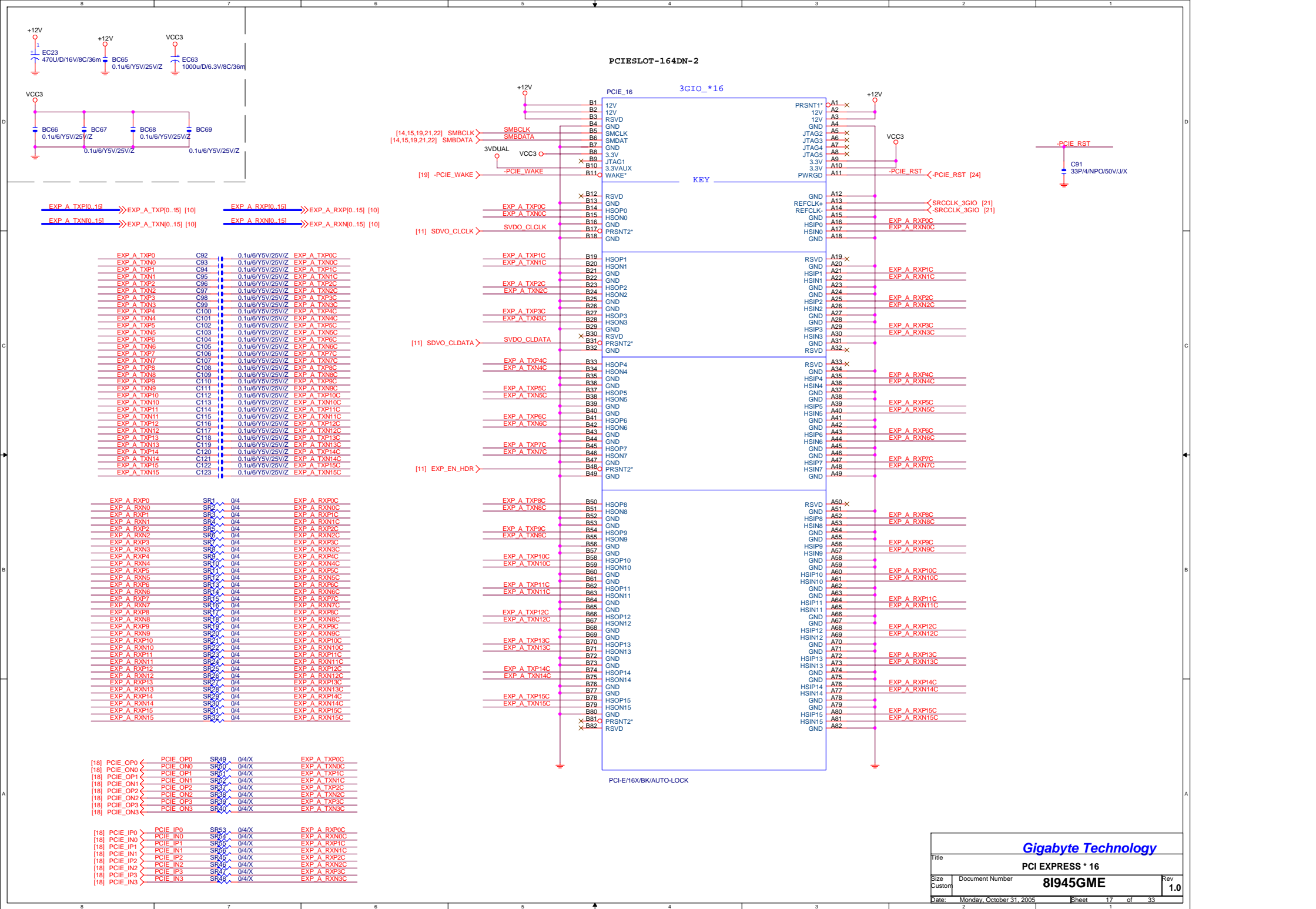
DDR18V Decouple

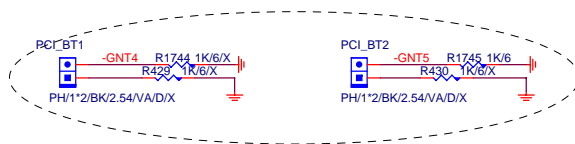
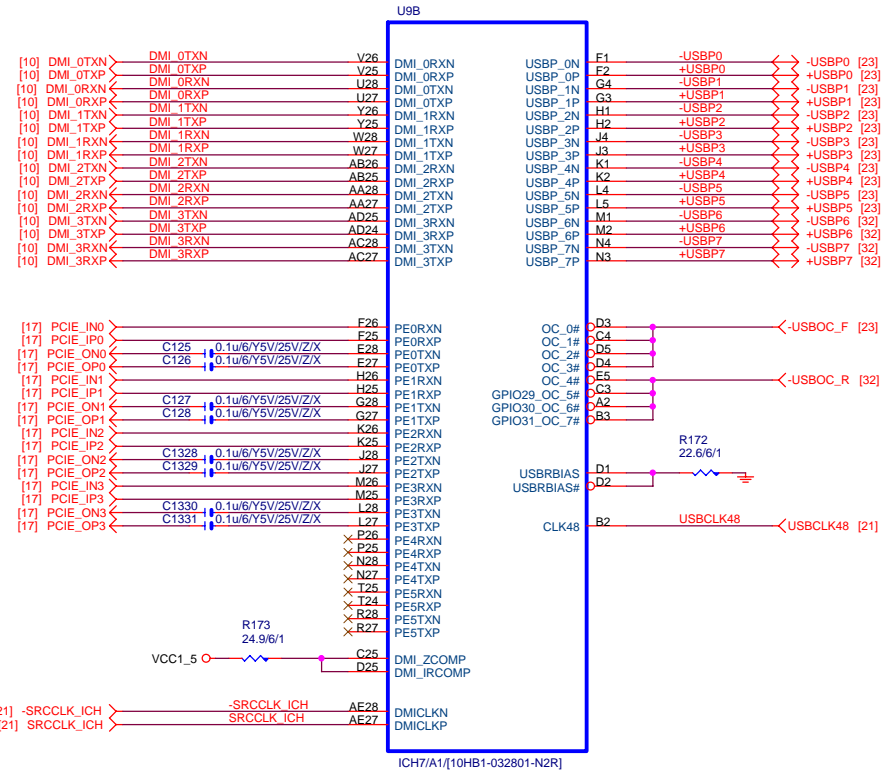
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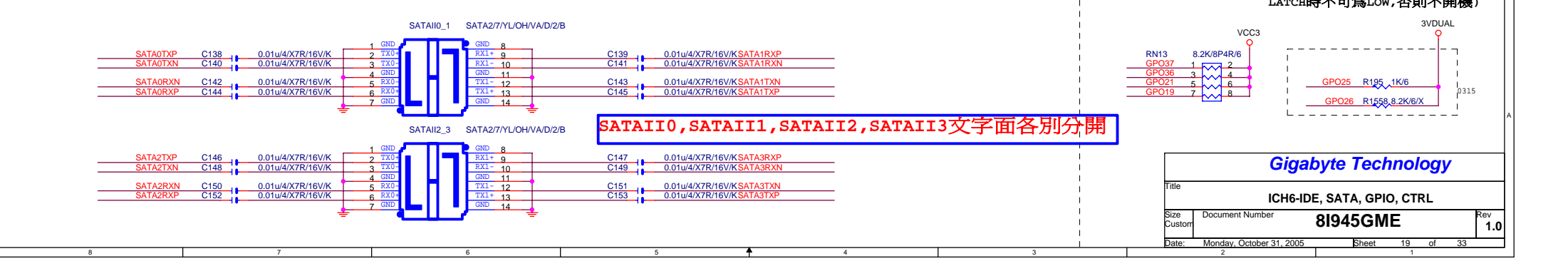
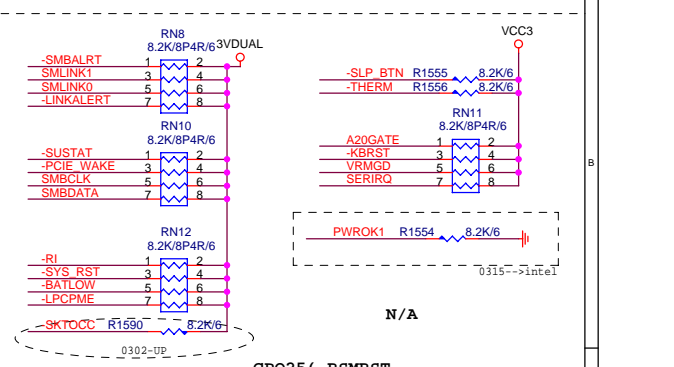
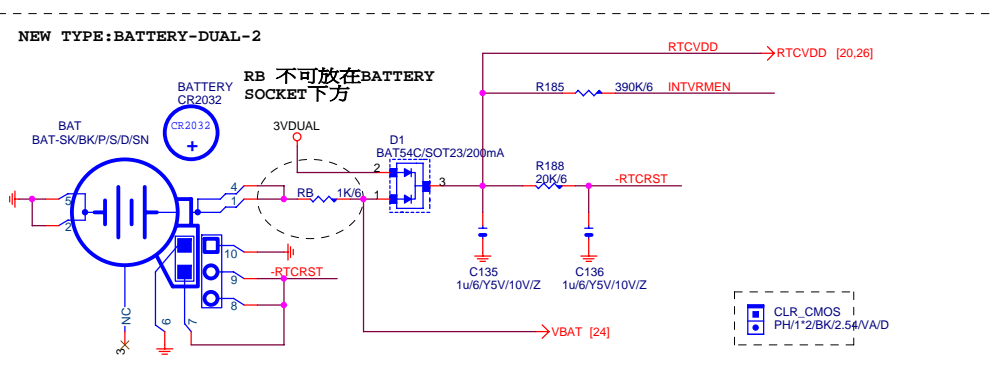
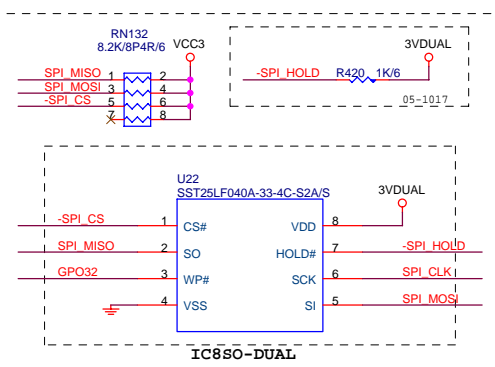
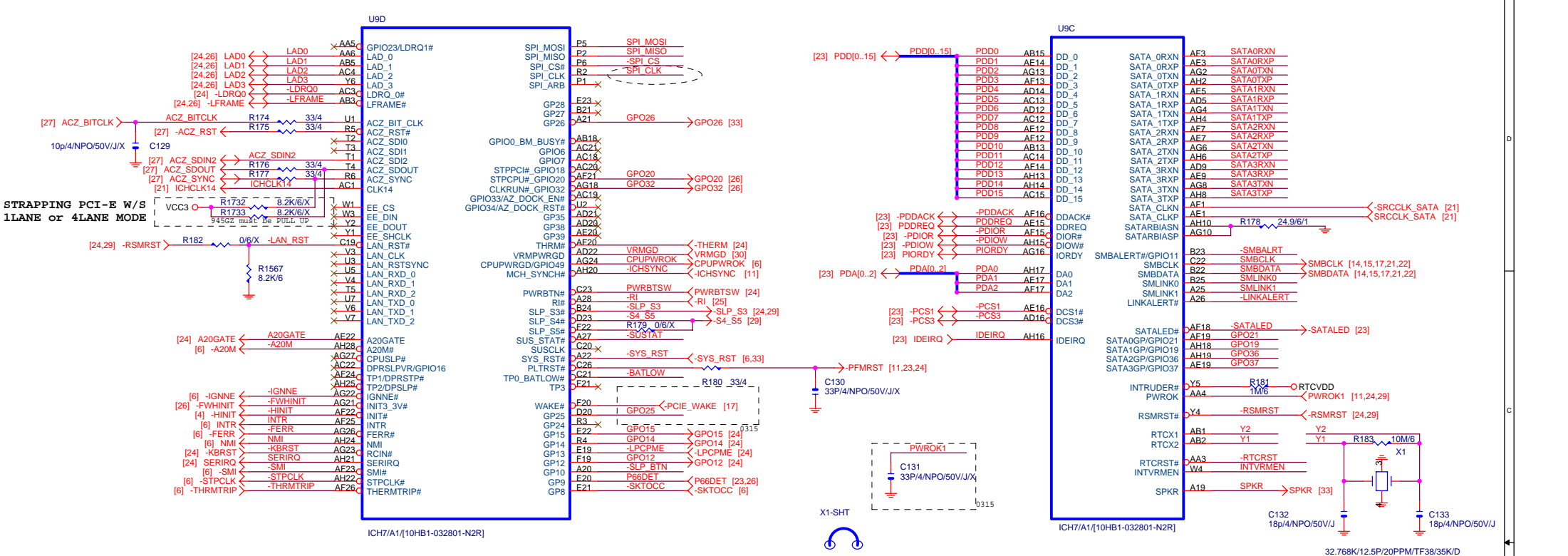


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Title			DDRII TERMINATOR
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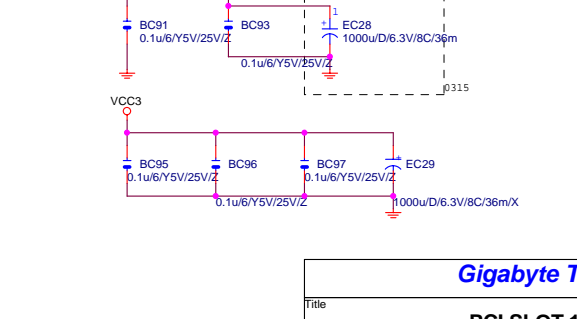
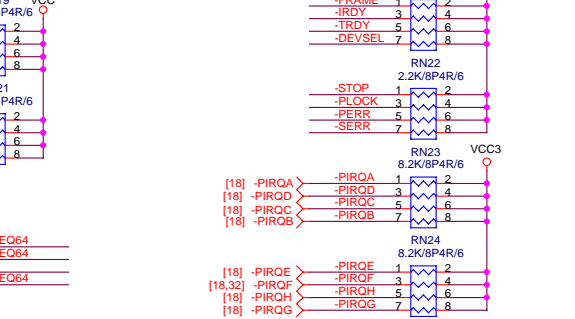
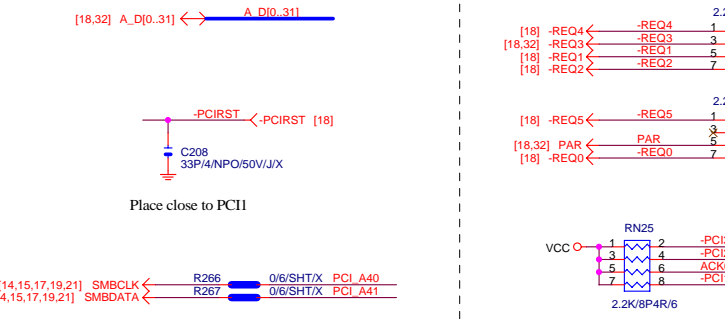
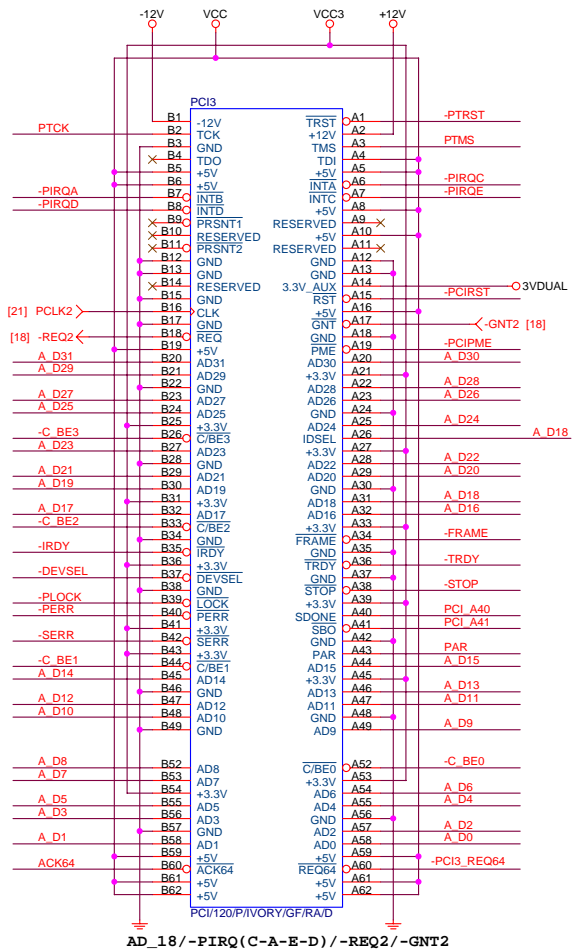
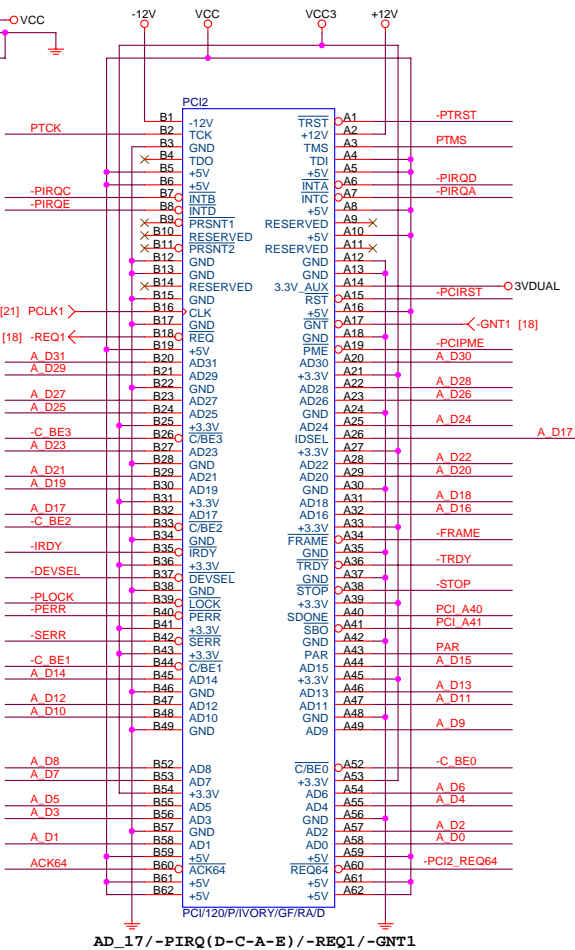
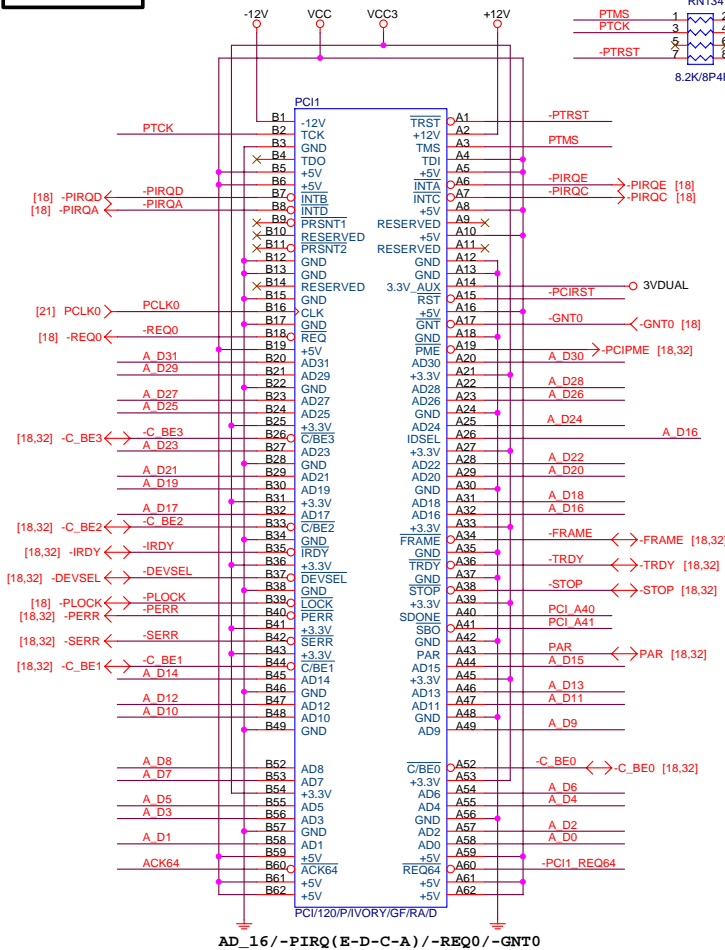




ICH6-PWR & GND

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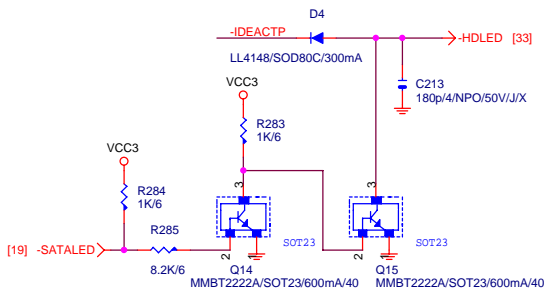
PCI1, 2 SLOT



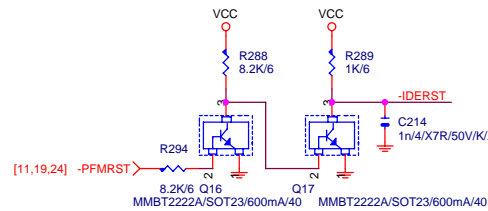
Gigabyte Technology

Title			
PCI SLOT 1, 2/PCIEX1			
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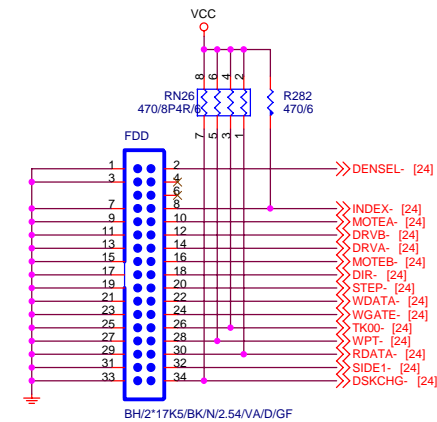
IDE/SATA LED



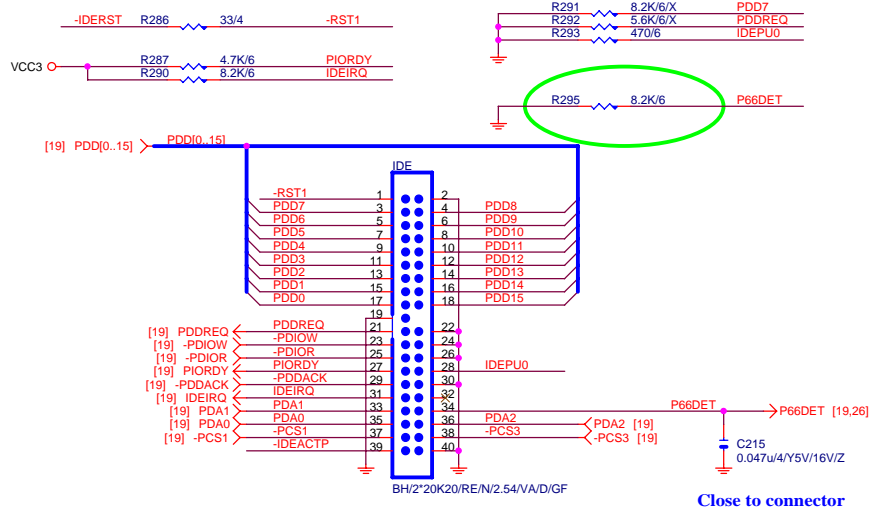
IDE RESET



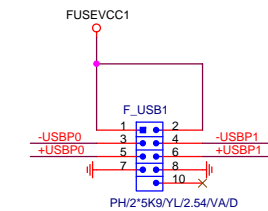
FLOPPY



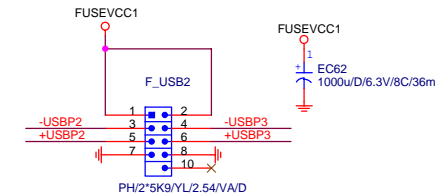
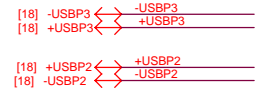
IDE



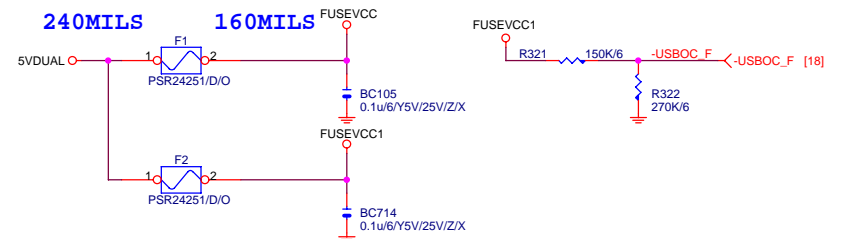
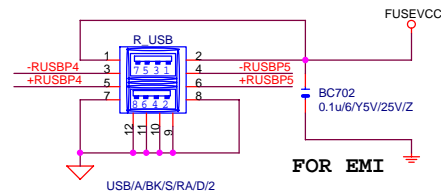
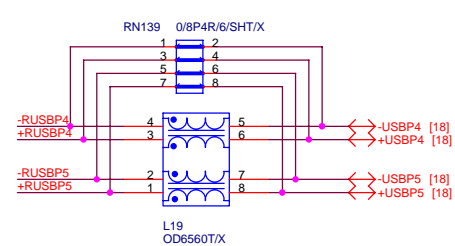
FRONT USB1



FRONT USB2

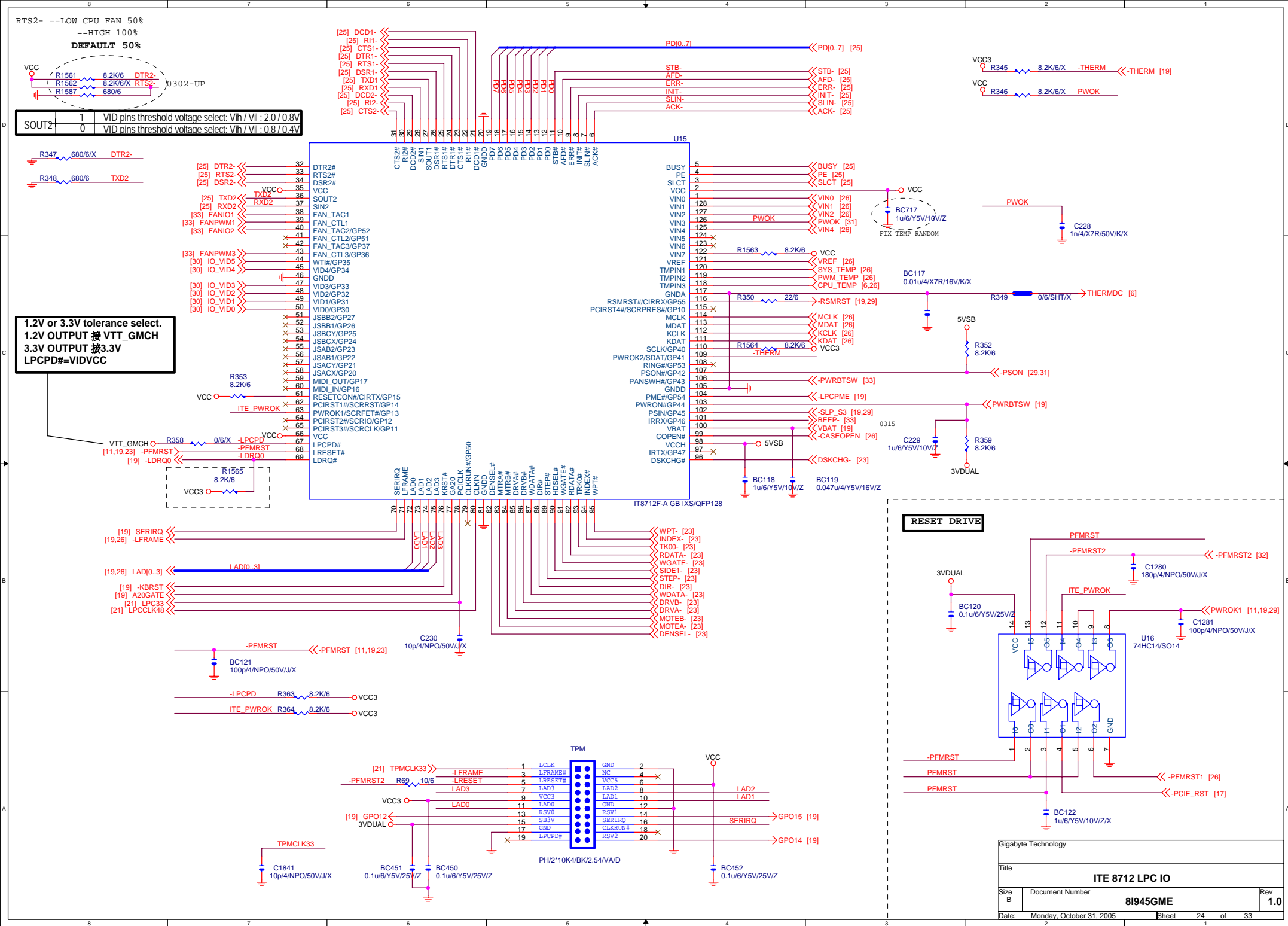


Close to connector

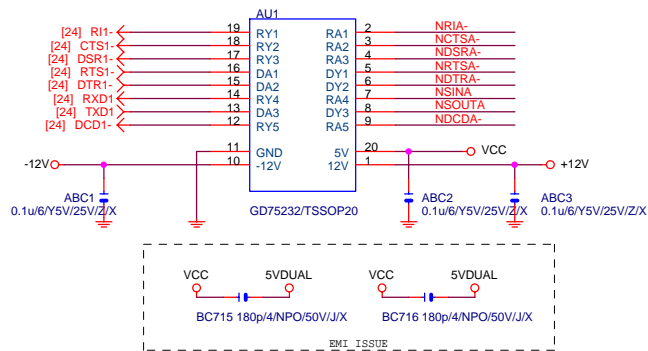


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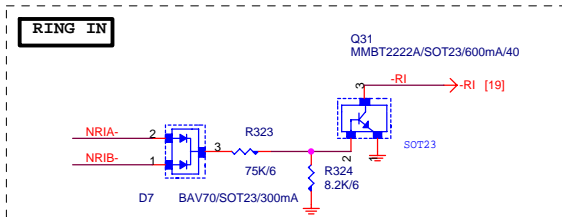
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IDE,FDD,F_USB			
Size			
B			
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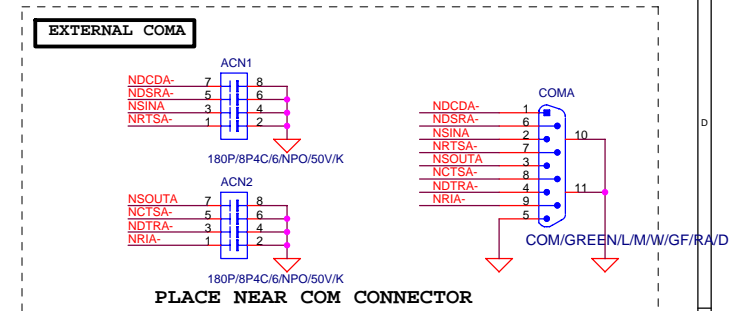
COMA



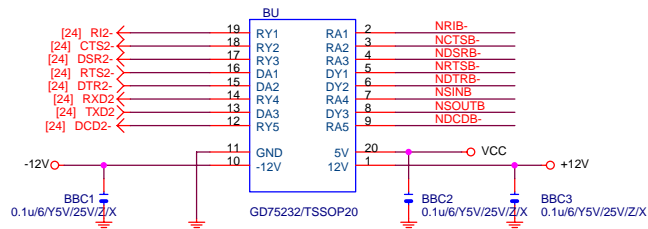
RING IN



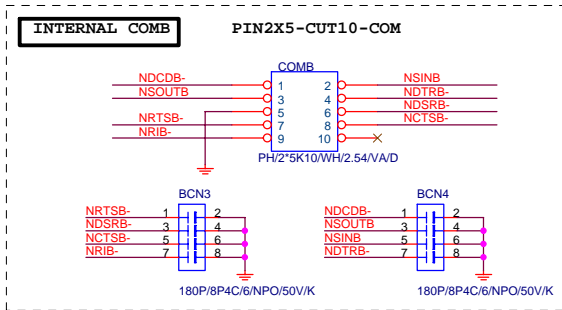
EXTERNAL COMA



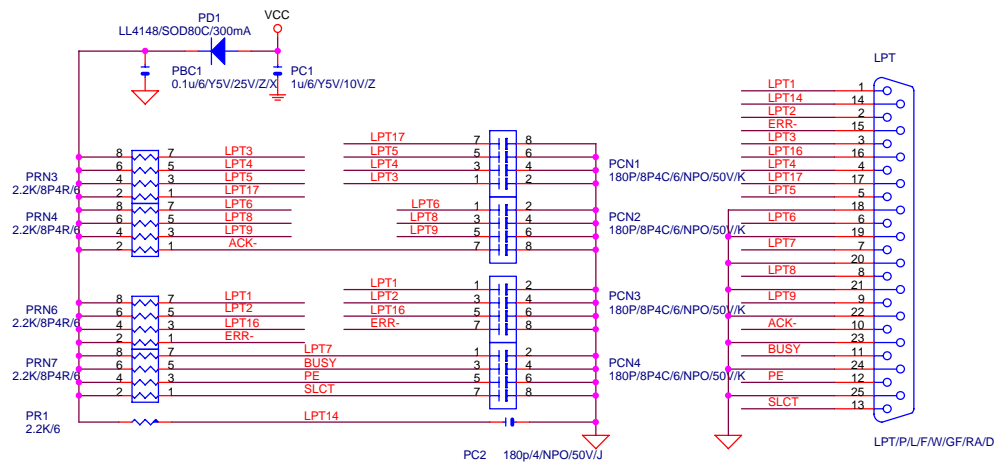
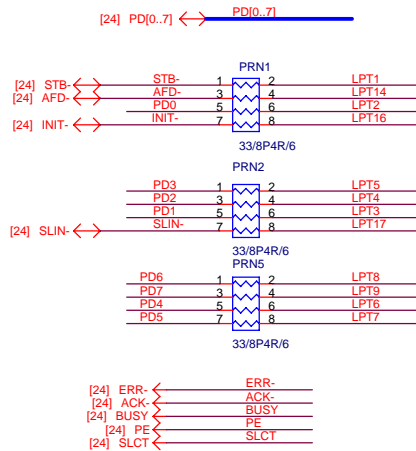
COMB



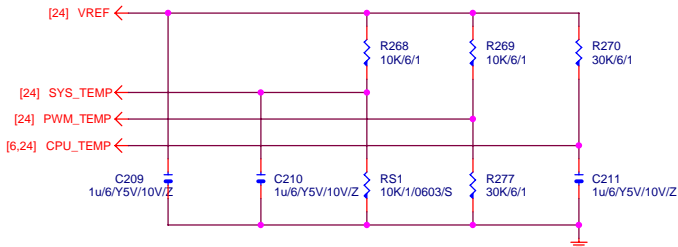
INTERNAL COMB



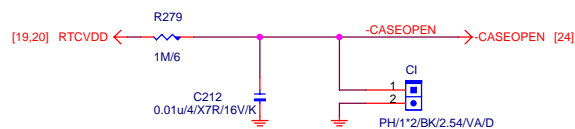
LPT PORT



TEMP H/W MONITOR

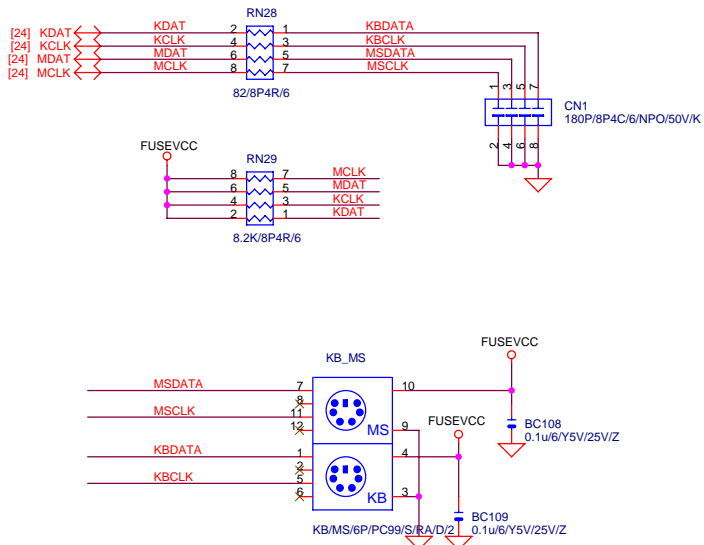


CASE OPEN

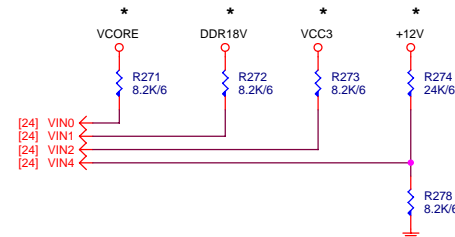


Case Open Circuits

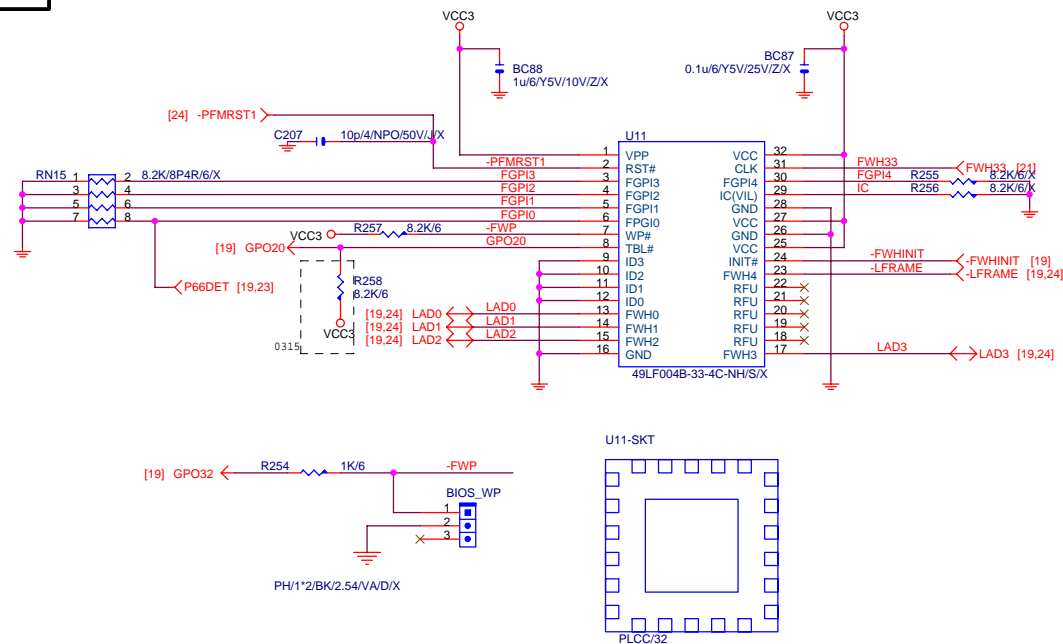
KB/MS



VOLTAGE-- H/W MONITOR

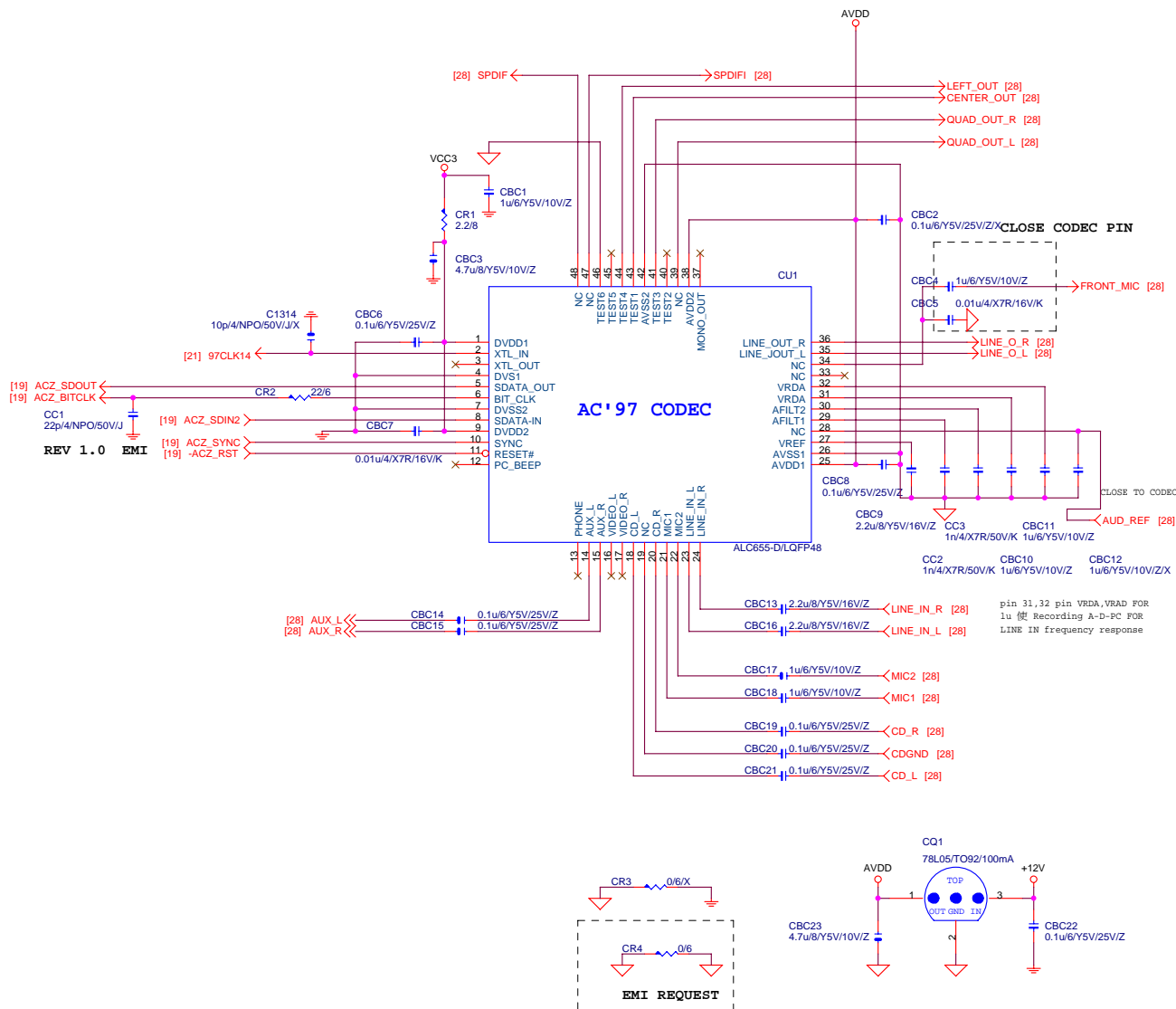


FWM BIOS



Gigabyte Technology

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BIOS/HW-MONITOR/CI/KB/MS		
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AUDIO (ALC655)			
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INTEL FRONT AUDIO

FOR EMI REQUEST

JP1/2'BLUE/GF/O::[5-6]CLOSE
JP1/2'BLUE/GF/O::[9-10]CLOSE

F_AUDIO

AVDD

CBC27
0.1u6/Y5V/25V/Z/X

CC7
180p/4/NPO/50V/J

CR11
8.2K/6

MIC1

FRONT_MIC

CR9
0/6/X

FLOR

Reserved

FLOL

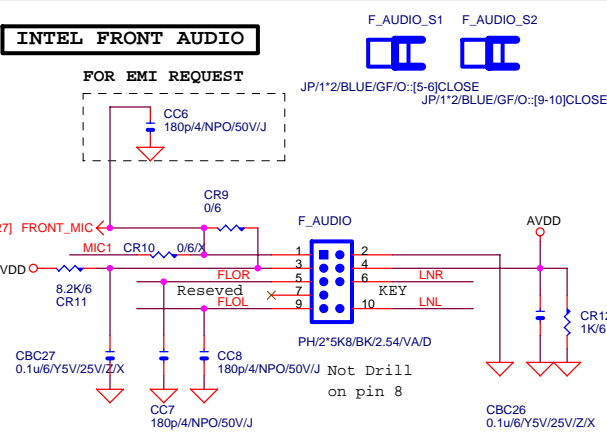
PH/2'S/K8/BK/2.54/VA/D

Not Drill on pin 8

CBC26
0.1u6/Y5V/25V/Z/X

CR1
1K/6

The schematic shows the front audio interface circuit. It includes a header JP1 with pins 5-6 and 9-10 closed. The F_AUDIO connector has 10 pins. Pin 1 is connected to MIC1, which goes to the FRONT_MIC pin. Pin 2 is connected to AVDD. Pin 3 is connected to FLOR. Pin 4 is connected to LNR. Pin 5 is connected to Reserved. Pin 6 is connected to FLOL. Pin 7 is connected to PH/2'S/K8/BK/2.54/VA/D. Pin 8 is labeled 'Not Drill on pin 8'. Pin 9 is connected to KEY. Pin 10 is connected to LNL. The circuit also includes capacitors CBC27, CC7, and CBC26, and resistors CR11, CR9, and CR1.



CD_IN

[27] CD_L ←

[27] CD_R ←

[27] CDGND ←

CC11

CC12

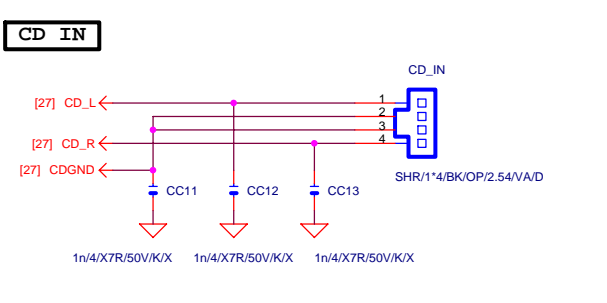
CC13

SHR/1*4/BK/OP/2.54/VA/D

1n4/X7R/50V/K/X

1n4/X7R/50V/K/X

1n4/X7R/50V/K/X



AUX IN

AUX_IN

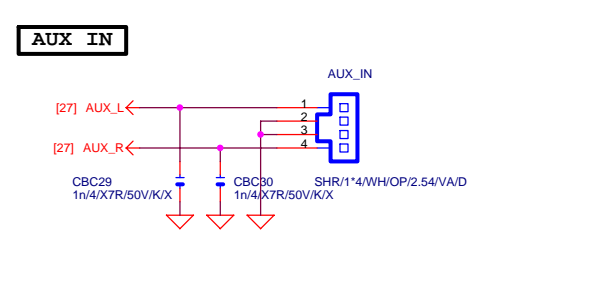
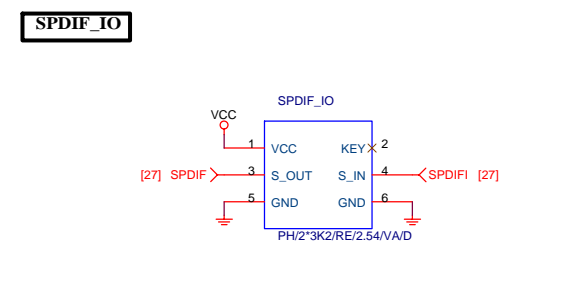
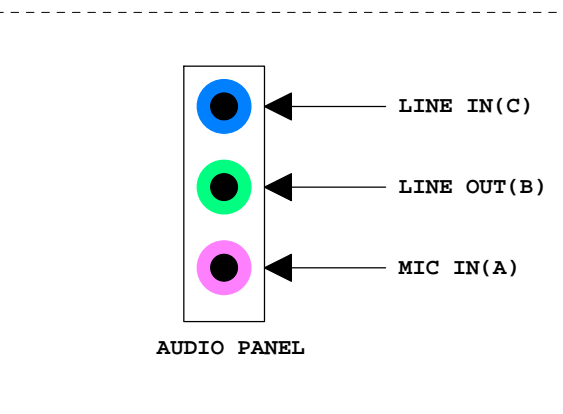
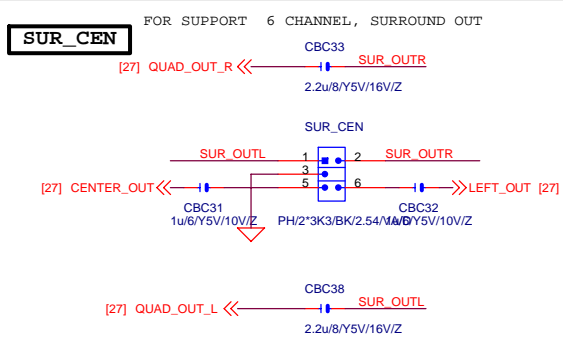
[27] AUX_L ←

[27] AUX_R ←

CBC29
1n4/X7R/50V/K/X

CBC30
1n4/X7R/50V/K/X

SHR/1*4/WH/OP/2.54/VA/D

[illegible]

LINE OUT

REV 1.0

CR6 0/6/X

CR8 0/6/X

CR5 22/6

CR7 22/6

CBC24 10u/8/Y5V/10V/Z

CBC25 10u/8/Y5V/10V/Z

CC4 180p/4/NPO/50V/J

CC5 180p/4/NPO/50V/J

3RP/13P/1/A/B/L/P/GF/RA/D

AUDIOB

B5

B4

B3

B2

LINE_O_R

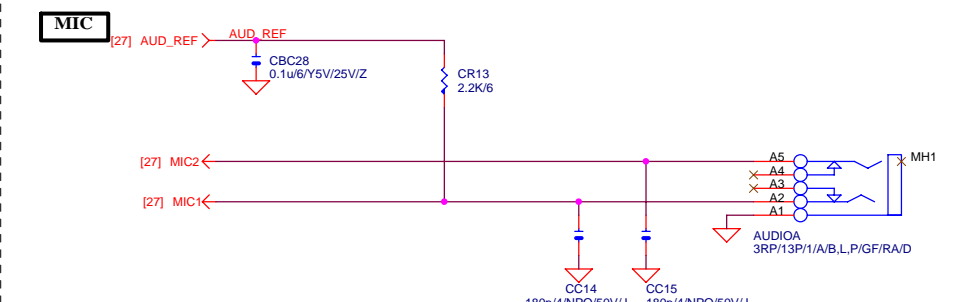
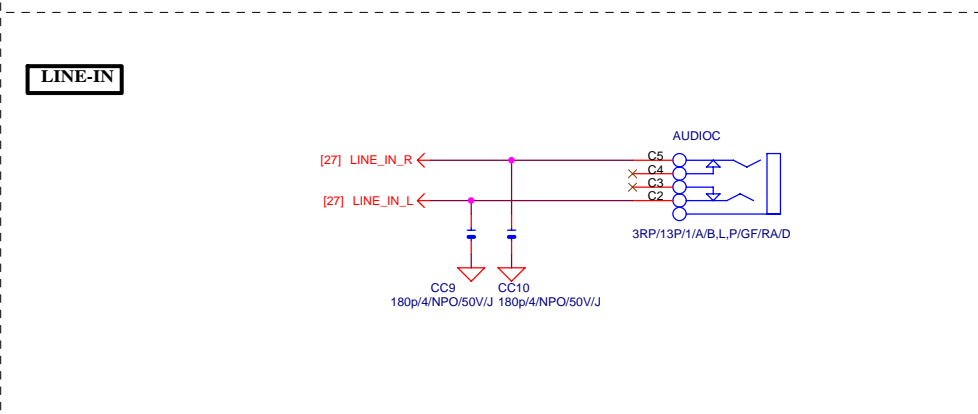
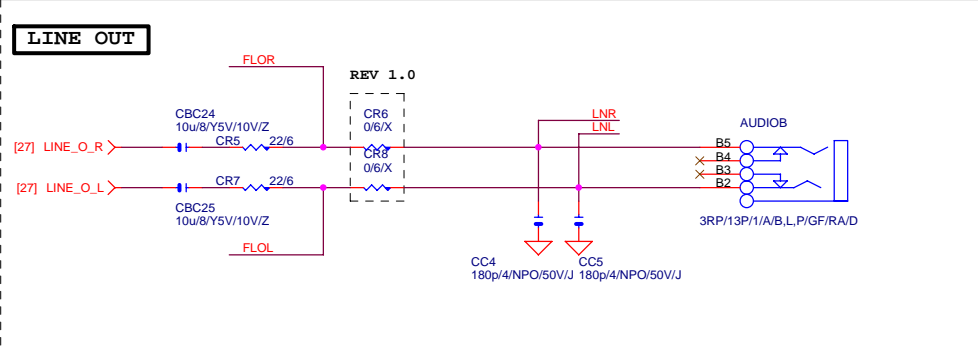
LINE_O_L

FLOOR

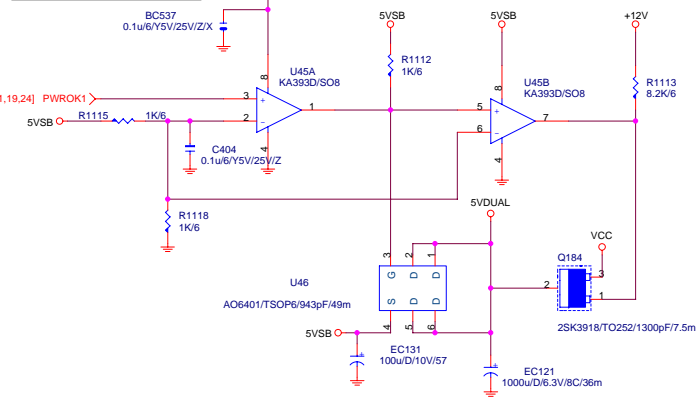
FLOL

LNR

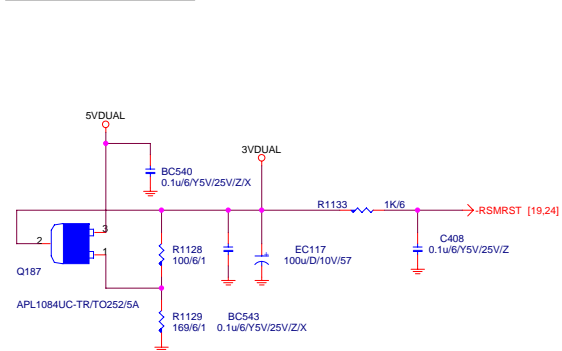
LNL



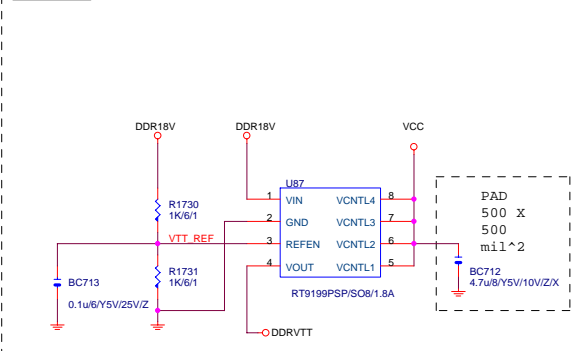
5VDUAL CIRCUIT



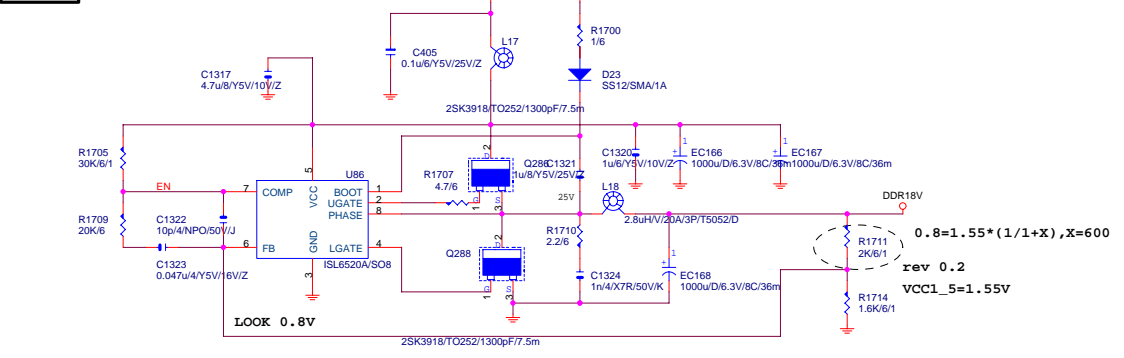
3VDUAL CIRCUIT



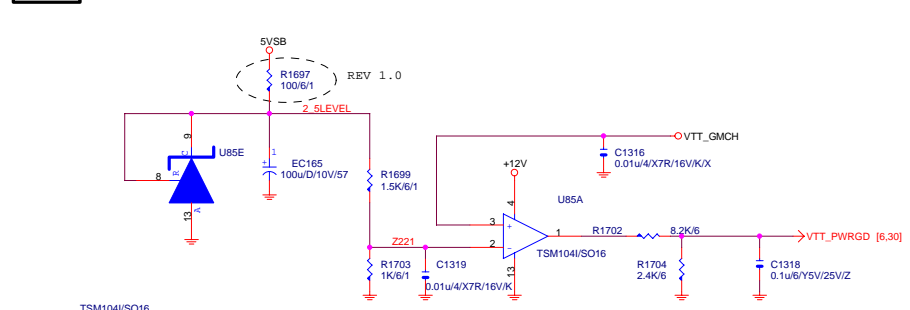
DDRVTT



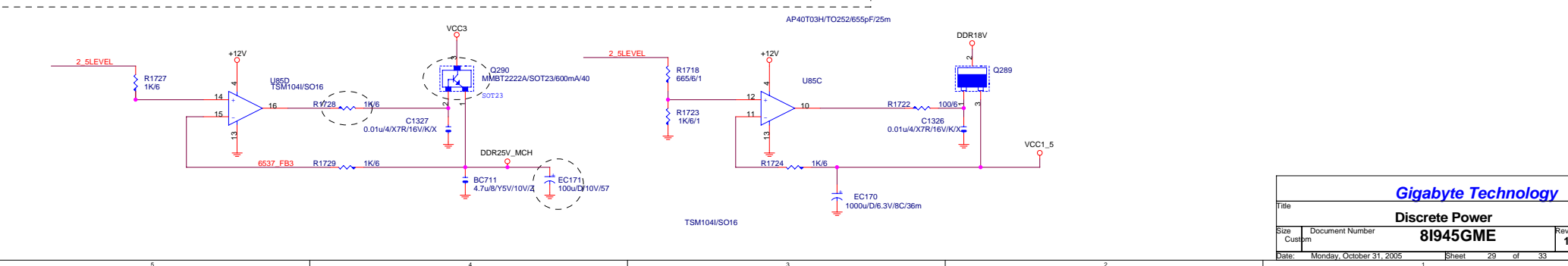
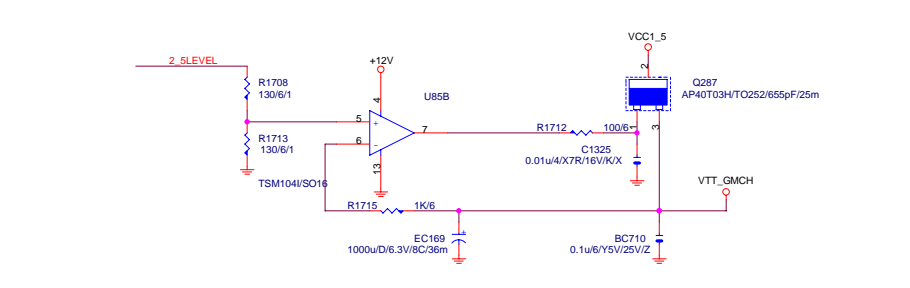
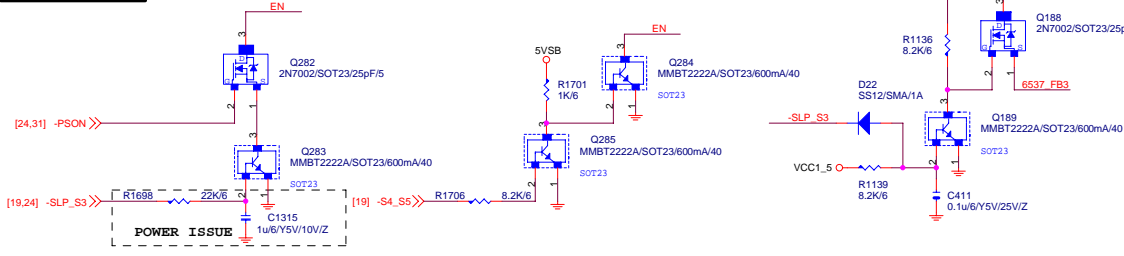
DDR18V



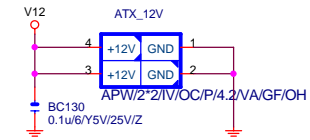
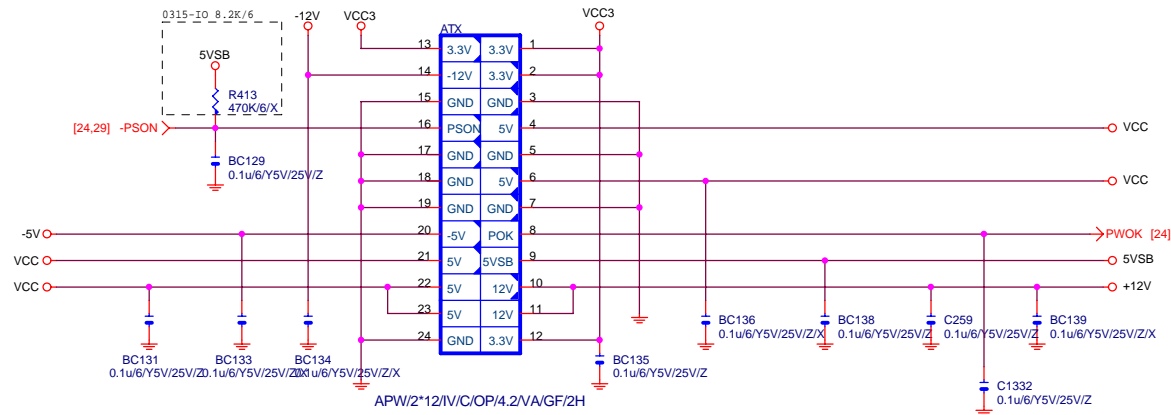
POWER



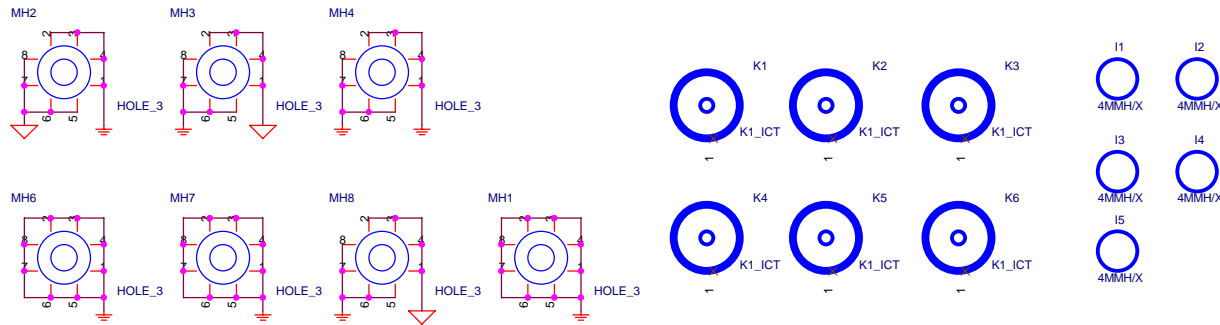
POWER SEQUENCY



ATX POWER CONNECTOR



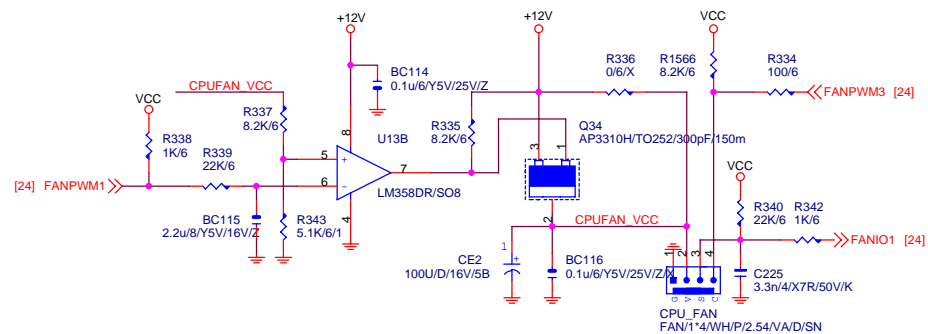
HOLE_3-2--->有鉛



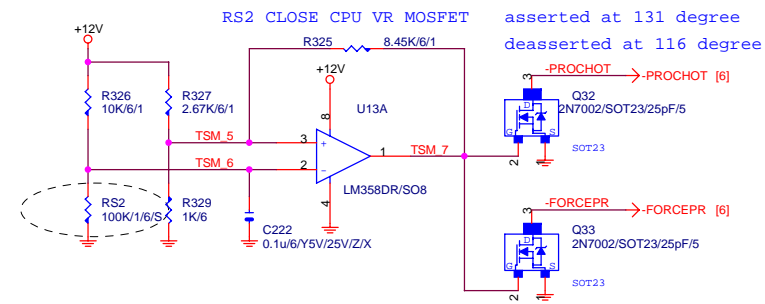
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Title			ATX POWER CONNECTOR
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	2	1	1.0

CPU SMART FAN SMART FAN

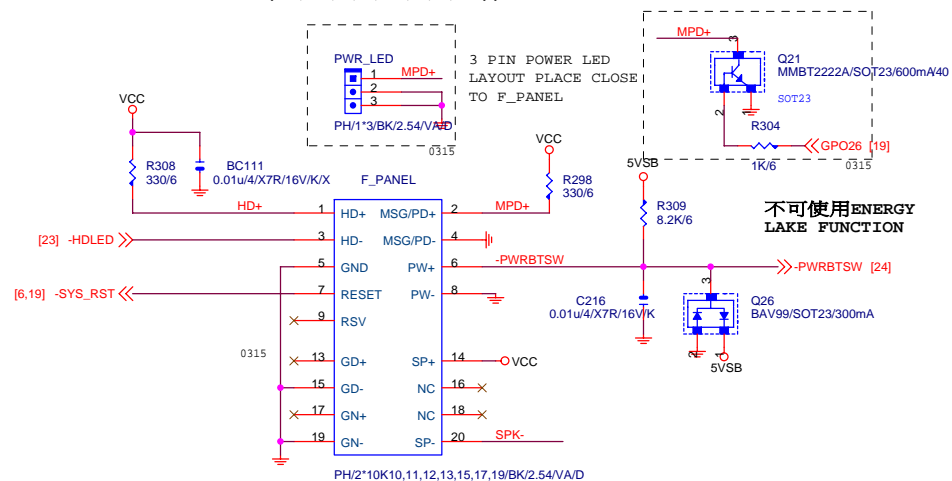


PROCESSOR HOT

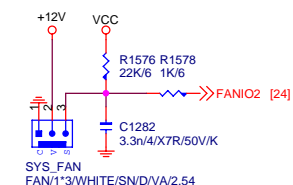


INTEL FRONT PANEL

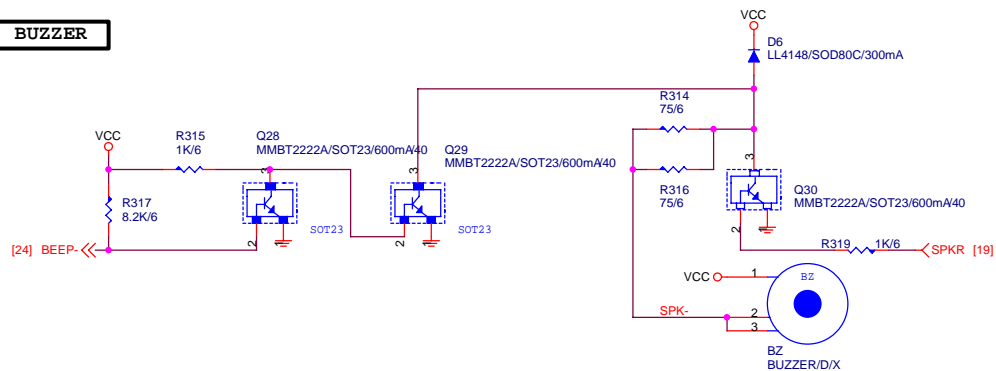
MPD- : (GPIO25--VCCSUS3+HI+HI+DEFINED(C3/C4/S/1/S3/S/4/S5)) -->INTEL



SYS_FAN



BUZZER



Gigabyte Technology

Title			
FRONT PANEL			
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